REMARKS

An Excess Claim Fee Payment Letter is submitted herewith to cover the cost of three (3) excess total claims.

Claims 3-25 are all the claims presently pending in the application. Claims 3, 8 and 22 have been amended to more particularly define the invention. Claims 23-25 have been added to claim additional features of the claimed invention.

It is noted that the claim amendments are made only for more particularly pointing out the invention, and not for distinguishing the invention over the prior art, narrowing the claims or for any statutory requirements of patentability. Further, Applicant specifically states that no amendment to any claim herein should be construed as a disclaimer of any interest in or right to an equivalent of any element or feature of the amended claim.

Claims 3-7, 14 and 18-21 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Iwata, et al. (U.S. Patent No. 5,880,500). Claims 8-13, 15-17 adn 22 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Iwata, et al. (U.S. Patent No. 5,880,500), in view of Wu (U.S. Patent No. 6,649,308).

These rejections are respectfully traversed in the following discussion.

I. THE CLAIMED INVENTION

The claimed invention (e.g., as claimed in claim 3) is directed to a method for manufacturing a semiconductor device (e.g., an n-type metal oxide semiconductor field effect transistor (NMOSFET)).

The method includes implanting n-type impurities within an NMOSFET forming region during a formation of channel regions and n-type source/drain regions, and implanting boron ions for forming a channel region to adjust threshold voltage within the NMOSFET forming region divided by an element dividing region, and implanting two different ions after the implantation of boron, including implanting arsenic ions in a semiconductor substrate at a first acceleration energy level which suppresses a reverse short channel effect to form arsenic ion implanted regions thereby forming the source/drain regions within the NMOSFET forming region, and after the implanting the arsenic ions, using a same photoresist mask as a photoresist mask used in implanting the arsenic ions, continuously implanting phosphorous ions in the arsenic ion implanted regions, at a second acceleration energy level lower than the

first acceleration energy level, so as to form a concentration peak of the phosphorous ions located in the arsenic ion implanted region, and performing a heat treatment to activate the arsenic ions and the phosphorous ions in the ion-implanted regions to form source/drain regions and buffer regions, the buffer regions including phosphorous ions and extending beyond the source/drain regions, thereby suppressing transient enhancement diffusion (TED) of a boron implanted region. The method also includes forming an NMOSFET having the source/drain.

Conventional methods of forming source/drain regions in a semiconductor device (e.g., an NMOSFET) include implanting arsenic at a high acceleration energy of about 50 keV in the source/drain region. However, as channel length and source/drain regions have become smaller, a reverse short channel effect has been realized in which the threshold voltage fluctuates largely for with a change in the length of the gate. The acceleration energy of implantation could be lowered to eliminate this reverse short channel effect, but this would result in an undesirable increase in p-n junction leakage current.

The claimed method, on the other hand, implants arsenic ions and, after the implanting the arsenic ions, using a same photoresist mask as a photoresist mask used in implanting the arsenic ions, continuously implants phosphorous ions in the arsenic ion implanted regions, at a second acceleration energy level lower than the first acceleration energy level, so as to form a concentration peak of the phosphorous ions located in the arsenic ion implanted region, and performing a heat treatment to activate the arsenic ions and the phosphorous ions in the ion-implanted regions to form source/drain regions and buffer regions, the buffer regions including phosphorous ions and extending beyond the source/drain regions, thereby suppressing transient enhancement diffusion (TED) of a boron implanted region.

As discussed in the Application at page 18, lines 20-25, and illustrated at Figure 10I, this feature allows the claimed invention to conveniently form the source/drain main region 46 and source/drain buffer region 48.

II. THE ALLEGED PRIOR ART REFERENCES

A. Iwata

The Examiner alleges that Iwata makes obvious the invention of claims 3-7, 14 and

18-21. Applicant submits, however, that there are elements of the claimed invention that are not taught or suggested by Iwata.

Iwata discloses a method of forming a semiconductor device in which phosphorous is implanted in a silicon substrate to form a first impurity diffusion region, and arsenic is later implanted to form a second impurity diffusion region (Iwata at Figure 1; col. 10, line 57-col. 11, line 15). Specifically, Iwata discloses a method in which first impurity regions 105 are formed by implanting phosphorous ions at an acceleration energy of 10-30 keV (Iwata at col. 11, lines 1-15). Thereafter, the impurities are activated at 850 to 900 EC (Iwata at col. 11, lines 59-64). Thereafter, third impurity regions 108 are formed by implanting arsenic ions at 20-40 keV (Iwata at col. 12, lines 34-40).

However, Iwata does not teach or suggest a method of forming a semiconductor device in which arsenic is implanted at a first acceleration energy (e.g., to form source/drain regions) and (e.g., after implanting the arsenic ions), *"using a same photoresist mask as a photoresist mask used in said implanting said arsenic ions, continuously implanting phosphorous ions in the arsenic ion implanted regions..."*, as recited in claim 3 and similarly recited in claims 8 and 22.

As noted above, this allows the claimed invention to conveniently form the source/drain main region 46 and source/drain buffer region 48 (Application at page 18, lines 20-25; Figure 10I).

This feature is clearly not taught or suggested by Iwata. Indeed, Iwata clearly teaches that phosphorus and arsenic are implanted in different steps. This is clearly illustrated, for example, in Figures 6(f)-6(k) in Iwata. Specifically, Figure 6(f) illustrates phosphorus ions 319 being implanted using photoresist 318 as a mask.

However, Iwata teaches that the photoresist 318 is thereafter removed and further processing is performed on the device (e.g., see Iwata at Figures 6(g)-6(j)). Then, **another photoresist (e.g., photoresist 329) which is different from the photoresist 318 used to implant the phosphorus, is formed and arsenic ions 330 are implanted**, as illustrated in Figure 6(k).

Thus, even assuming (arguendo) that Iwata teaches or suggests implanting phosphorus ions after implanting arsenic ions (which Applicant again reiterates is clearly not correct), Iwata clearly does not teach or suggest (after implanting arsenic ions), using the same

photoresist mask as a photoresist mask used in implanting the arsenic ions, continuously implanting phosphorous ions in the arsenic ion implanted regions. Thus, Iwata teaches a method that is less convenient and completely unrelated to the claimed invention.

Further, Applicant notes that in the claimed invention, aresenic ions are implanted in a low implantation energy level (e.g., to suppress the **reverse** short channel effect). Thereafter using a same photoresist mask as a photoresist mask used in implanting the arsenic ions, continuously phosphorus ions are implanted at a low implantation energy which is lower than the implantation energy of arsenic ions to form a concentration peak region of implanted ions within the arsenic ion implanted region.

Further, heat treatment may be performed on the ion implanted regions for activation of the arsenic ions and phosphorus ions to form source/drain regions, thereby providing a NMOSFET having a suppressed **reverse** short channel effect, and a suppressed transient enhancement diffusion (TED) of the boron.

As Applicant has previously pointed out to the Examiner, but to which the Examiner has never responded, Iwata is not intended to address the problem of reverse short channel effect, but instead merely teaches to protect from the short channel effect, which is not the same as a reverse short channel effect.

Further, Iwata clearly does not teach or suggest an object of the structure of the claimed invention which may suppress the transient enhancement diffusion (TED) of the boron implanted in the channel region, and which may also suppress the reverse channel effect.

Therefore, it is clear that Iwata is completely unrelated to the claimed invention.

Therefore, Applicant submits that Iwata does not teach or suggest each and every element of the claimed invention. Therefore, the Examiner is respectfully requested to withdraw this rejection.

B. Wu

The Examiner alleges that Iwata makes obvious the invention of claims 8-13, 15-17 and 22. Applicant submits, however, that these references would not have been combined and even if combined, the combination would not teach or suggest each and every element of the claimed invention.

Wu discloses an ultra-short channel transistor in a semiconductor substrate includes a gate structure that is formed on the substrate. Side-wall spacers are formed on the side walls of the gate structure as an impurities-diffusive source. Source and drain regions are formed in the substrate. A metal silicide contact is formed on the top surface of the gate structure, and on the surface of the source and drain regions. Extended source and drain regions are formed beneath the side-wall spacers and connect next to the source and drain regions.

However, Applicant submits that these references would not have been combined as alleged by the Examiner. Indeed, these references are directed to different problems and solutions.

Specifically, in contrast Iwata which teaches to suppress a short-channel effect by making a shallow second impurity diffusion layer (Iwata at col. 4, lines 39-32), Wu teaches to suppress a short-channel effect by forming an extended ultra-shallow S/D junction using a PSG or BSG film as a diffusion source (Wu at col. 5, lines 1-4). Therefore, these references are completely unrelated, and no person of ordinary skill in the art would have considered combining these disparate references, absent impermissible hindsight.

Further, Applicant submits that the Examiner can point to no motivation or suggestion in the references to urge the combination as alleged by the Examiner. Indeed, contrary to the Examiner's allegations, neither of these references teach or suggest their combination. Therefore, Applicant respectfully submits that one of ordinary skill in the art would not have been so motivated to combine the references as alleged by the Examiner. Therefore, the Examiner has failed to make a prima facie case of obviousness.

Moreover, Applicant respectfully submits that neither Iwata, nor Wu, nor any combination thereof teaches or suggests a method of forming a semiconductor device in which arsenic is implanted at a first acceleration energy (e.g., to form source/drain regions) and (e.g., after implanting the arsenic ions), *"using a same photoresist mask as a photoresist mask used in said implanting said arsenic ions, continuously implanting phosphorous ions in the arsenic ion implanted regions..."*, as recited in claim 3 and similarly recited in claims 8 and 22.

As noted above, this allows the claimed invention to conveniently form the source/drain main region 46 and source/drain buffer region 48 (Application at page 18, lines 20-25; Figure 10I).

Clearly, these features are not taught or suggested by Wu. Indeed, the Examiner merely relies on Wu as allegedly teaching implanting arsenic at a specific acceleration energy (Office Action at page 3).

Nowhere does Wu teach or suggest implanting phosphorus ions after implanting the arsenic ions. Moreover, Wu certainly does not teach or suggest (e.g., after implanting the arsenic ions) continuously implanting phosphorous ions in the arsenic ion implanted regions **using a same photoresist mask as a photoresist mask used in implanting the arsenic ions**, as in the claimed invention.

Further, like Iwata, Wu is not intended to address the problem of reverse short channel effect, but instead merely teaches to protect from the short channel effect, which is not the same as a reverse short channel effect. Further, like Iwata, Wu clearly does not teach or suggest an object of the structure of the claimed invention which may suppress the transient enhancement diffusion (TED) of the boron implanted in the channel region, and which may also suppress the reverse channel effect.

Therefore, Applicant submits that these references would not have been combined and even if combined, the combination would not teach or suggest each and every element of the claimed invention. Therefore, the Examiner is respectfully requested to withdraw this rejection.

III. FORMAL MATTERS AND CONCLUSION

In view of the foregoing, Applicant submits that claims 3-25, all the claims presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Attorney's Deposit Account No. 50-0481.

Respectfully Submitted,

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